CENG 450

Post-lab Summary

February 4th, 2014

Lab Session 2

Lab session 2 revolved around the design of the registers and the ALU. Skeleton code was provided for the register unit, while the ALU was written from scratch.

The skeleton code for the registers set up the inputs and outputs of the unit. These consisted of two data and address busses to read, and data and address to write, as well as the mode select, reset ad clock. In addition, the code provided the reset algorithm and the *read* and *write* cases. We were left to fill in the *write* case by using a *case* statement using the *wr\_index* as input. Each case wrote the data to the corresponding location in *reg\_array*. We also filled in the in the code for outputting data to *rd\_data2* by using the *when/else* statement taking input from the *rd\_index2* bus.

With the code filled in, the simulation showed that data written to a certain register in memory could be read from that register later.

The ALU code was written from scratch, using Table V in the Instruction Set document as reference. The ALU code we wrote consisted of a series of *if* statements, each controlling a different op code on the *alu­\_mode* bus. Once the task was performed, the output was put on the result bus directly, without waiting for the clock pulse. On the clock pulse, however, the N and Z flags are loaded on to their output pins.